

Patent claims

1. A semiconductor component comprising a stack (100)
of semiconductor chips (1, 2), the semiconductor
5 chips (1, 2) of the semiconductor chip stack (100)
being arranged in a manner fixed cohesively one on
top of another, and the semiconductor chips (1, 2)
comprising contact areas (5) extending as far as
the edges (6) of the semiconductor chips (1, 2),
10 and conductor portions (7) extending from at least
one upper edge (8) to a lower edge (9) of the edge
sides (10) of the semiconductor chips (1, 2) and
electrically connecting the contact areas (5) of
the semiconductor chips (1, 2) of the
15 semiconductor chip stack (100).
2. The semiconductor component as claimed in claim 1,
characterized in that
the semiconductor chips (1, 2) have different chip
20 sizes.
3. The semiconductor component as claimed in claim 1
or claim 2,
characterized in that
25 the semiconductor chips (1, 2) have a different
number of contact areas (5) at their edges (6).
4. The semiconductor component as claimed in one of
the preceding claims,
30 characterized in that
the electrically conductive conductor portions (7)
are arranged adhesively on the semiconductor chip
edges (6), the semiconductor edge sides (10), the
semiconductor top side (11) and/or the
35 semiconductor rear side (12) with a freely
selectable stacking order.
5. The semiconductor component as claimed in one of

- the preceding claims,
characterized in that
the conductor portions (7) comprise an adherent
plastic resist which is filled with metallic
nanoparticles and is electrically conductive.
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6. The semiconductor component as claimed in claim 4
or claim 5,
characterized in that
the nanoparticle-filled plastic resist is soluble
in a solvent.
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7. The semiconductor component as claimed in one of
the preceding claims,
characterized in that
the nanoparticle-filled plastic resist can be
patterned by means of laser removal.
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8. The semiconductor component as claimed in one of
the preceding claims,
characterized in that
the nanoparticle-filled plastic resist can be
patterned photolithographically.
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9. The semiconductor component as claimed in one of
the preceding claims,
characterized in that
the semiconductor chip stack (100) comprises a
multilayer rewiring layer comprising nanoparticle-
filled electrically conductive patterned plastic
resist layers (15) and insulation layers (16, 17)
arranged in between on the edge sides (10) of the
semiconductor chips (1, 2).
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- 30
- 35
10. A method for producing a semiconductor component
comprising a stack (100) of semiconductor chips
(1, 2) the method having the following method
steps of:

- producing semiconductor chips (1, 2) with contact areas (5) extending as far as the edges (6) of the semiconductor chip (1, 2),
 - cohesively fixing the semiconductor chips (1, 2) one above another to form a semiconductor stack (100),
 - encapsulating the semiconductor stack (100) with a layer (15) made of a plastic resist which is filled with nanoparticles,
 - patterning the layer (15) to form interconnect sections (7) between the contact areas (15) of the semiconductor chips (1, 2) stacked one on top of another.
11. The method as claimed in claim 10, characterized in that the layer (15) made of plastic resist for encapsulating the semiconductor stack (100) is sprayed on.
12. The method as claimed in claim 10 or claim 11, characterized in that the semiconductor stack (100), for encapsulation with a layer (15) made of plastic resist, is dipped into a bath of nanoparticle-filled plastic resist.
13. The method as claimed in one of claims 10 to 12, characterized in that a laser removal method is effected for patterning the nanoparticle-filled plastic resist to form interconnect sections (7).
14. The method as claimed in one of claims 10 to 12, characterized in that a photolithography method is carried out for patterning the nanoparticle-filled layer (15) made of plastic resist to form interconnect sections

(7).

15. The method as claimed in one of claims 10 to 12,
characterized in that
5 the interconnect sections (7) are applied to the
semiconductor stack (100) selectively by means of
precision injection techniques.
16. The method as claimed in one of claims 10 to 15,
10 characterized in that
multilayer interconnect sections (7) in
alternation with insulation layers (16, 17) are
applied to the semiconductor stack (100).